CLAIMS

1. A method for processing a microelectronic substrate, comprising:

providing a microelectronic substrate having a first surface and a second surface facing a direction opposite from the first surface;

forming a plurality of voids in the microelectronic substrate, each void having an open end at the first surface and extending from the first surface to a separation region between the first and second surfaces;

forming at least one operable microelectronic device at and/or proximate to the first surface of the microelectronic substrate; and

separating a first stratum of the microelectronic substrate above the separation region from a second stratum of the microelectronic substrate below the separation region.

2. The method of claim 1, further comprising:

at least partially filling the voids with a filler material to close the open end of the voids;

constructing a film on the first surface of the first substrate; and

forming at least one operable microelectronic device in the film.

3. The method of claim 1 wherein forming the voids includes forming tapered voids having a first void area transverse to the first surface of the substrate at the first surface and a second void area transverse to the first surface of the substrate below the first surface, the second void area being larger than the first void area.

4. The method of claim 3 wherein forming the tapered voids includes disposing an etchant on the first surface of the substrate and tilting the substrate.

5. The method of claim 3 wherein forming the tapered voids includes directing an energy beam toward the first surface of the substrate and tilting the substrate as the energy beam impinges on the first surface.

6. The method of claim 1, further comprising forming each of the voids to have approximately the same depth beneath the first surface so that the separation region is generally flat.

7. The method of claim 1, further comprising closing entrance openings of the voids at the first surface of the substrate by at least partially filling the voids.

8. The method of claim 1 wherein the substrate includes a die having a transverse dimension at the first surface, further comprising spacing adjacent voids by a distance less than the transverse dimension.

9. The method of claim 1 wherein separating the first stratum of the microelectronic substrate from the second stratum includes applying a force to the first stratum in a selected direction to break connecting portions of the microelectronic substrate coupling the first and second strata of the microelectronic substrate between the voids.

10. The method of claim 9, further comprising varying a magnitude of the force while engaging the first stratum of the microelectronic substrate.

11. The method of claim 9 wherein the separation region defines a plane and applying a force includes applying a force in a direction parallel to the plane.

12. The method of claim 9 wherein the separation region defines a plane and applying a force includes applying a force in a direction transverse to the plane.

13. The method of claim 9, further comprising releasably engaging the first surface of the microelectronic substrate by applying a suction force to the first surface.

14. The method of claim 1 wherein forming at least one microelectronic device includes forming first microelectronic devices defining a first microelectronic die and forming second microelectronic devices defining a second microelectronic die.

15. The method of claim 1, further comprising selecting the substrate to include silicon.

16. The method of claim 1, further comprising selecting the substrate to include a wafer.

17. The method of claim 16, further comprising selecting the wafer to have a diameter of from about eight inches to about twelve inches.

18. The method of claim 1, further comprising venting gases through the voids.

19. The method of claim 1, further comprising aligning the voids along a line separating adjacent dies.

20. The method of claim 1, further comprising merging at least a portion of one void with a portion of an adjacent void.

21. The method of claim 1, further comprising at least partially separating a first die of the substrate from an adjacent second die of the substrate by aligning the voids between the dies.

22. A method for forming a plurality of microelectronic dies, comprising:

providing a substrate having a first surface and a second surface facing a direction opposite the first surface;

perforating the substrate at a separation region by forming a plurality of voids in the first substrate, the voids having an open end at the first surface with a first transverse dimension and a closed end at the separation region between the first and second surfaces, the closed end having a second transverse dimension greater than the first transverse dimension;

constructing a film on the first surface of the substrate;

forming a plurality of microelectronic devices in and/or on the film to define first and second microelectronic dies;

separating the first die from the second die by cutting through the film in a direction transverse to a plane of the separation region; and

separating the first and second dies from the substrate along the separation region.

23. The method of claim 22 wherein the substrate includes a first lattice structure and the film includes a second lattice structure, further comprising aligning the second lattice structure with the first lattice structure.

24. The method of claim 22, further comprising selecting the film to have a chemical composition the same as a chemical composition of the substrate.

25. The method of claim 22 wherein separating the first die from the second die includes disposing a blade between the first and second dies.

26. The method of claim 22 wherein the first die separates from the second die before the first and second dies separate from the substrate.

27. The method of claim 22, further comprising closing the open ends of the voids at the first surface of the substrate by at least partially filling the voids before disposing the film on the substrate.

28. The method of claim 22 wherein separating the first die from the second die includes merging voids positioned between the first and second dies.

29. The method of claim 22 wherein separating the first and second dies from the substrate includes applying a suction cup to the first die, at least partially evacuating the suction cup, and applying a force to the first die in a selected direction to break connecting portions of the substrate coupling the die to the substrate between the voids.

30. The method of claim 29, further comprising varying a magnitude of the force while engaging the first die.

31. The method of claim 29 wherein applying a force includes applying a force transverse to a plane of the separation region.

32. The method of claim 22, further comprising spacing the voids apart by a distance less than a transverse dimension of the first die.

33. A microelectronic die, comprising:

a substrate having a first external surface, a second external surface facing a direction opposite from the first external surface, and a thickness between the first and second external surfaces of less than about 150 microns; and

at least one operable microelectronic device at least proximate to one of the external surfaces.

34. The microelectronic die of claim 33 wherein the second external surface includes a plurality of blind voids extending from the second surface toward the first surface, the voids having an open end at the second surface and a closed end between the second and first surfaces.

35. The microelectronic die of claim 34 wherein the voids are etched voids.

36. A microelectronic die, comprising:

a substrate having a first external surface, a second external surface facing a direction opposite from the first external surface, and a plurality of voids extending from the second external surface toward the first external surface; and

a plurality of operable microelectronic devices proximate to the first surface.

37. The microelectronic die of claim 36, wherein the first external surface is separated from the second external surface by about 150 microns or less.

38. The microelectronic die of claim 36 wherein the voids are tapered and are larger toward the second external surface of the substrate than toward the first external surface.

39. The microelectronic die of claim 36 wherein the voids are etched voids.

40. The microelectronic die of claim 36 wherein the voids are regularly spaced apart from each other.

41. The microelectronic die of claim 39 wherein the voids are randomly spaced apart from each other.

42. A microelectronic substrate for forming one or more microelectronic dies, the substrate comprising:

a substrate body having a first surface and a second surface facing a direction opposite the first surface; and

a plurality of sidewalls in the substrate body, each sidewall defining a void within the substrate body, each void having a first end at the first surface of the substrate body and a second end at a separation region between the first and second surfaces of the substrate body.

43. The substrate of claim 42, further comprising at least one operable microelectronic device at and/or proximate to the first surface of the substrate body.

44. The substrate of claim 42 wherein each void is a blind void with the second end being a closed end, further wherein the first end of each void is filled with a filler material.

45. The substrate of claim 42 wherein the substrate body includes silicon.

46. The substrate of claim 42 wherein the substrate body includes a wafer having a diameter of from about eight inches to about twelve inches.

47. The substrate of claim 42, further comprising a film layer disposed on the first surface of the substrate body.

48. The substrate of claim 47 wherein the film has an external surface facing an opposite direction from the second surface of the substrate body, further wherein a distance between the external surface and the separation region is less than about 150 microns.

49. The substrate of claim 42 wherein the voids are tapered with the first end of each void smaller than the second end of each void.

50. The substrate of claim 42 wherein the voids include first and second voids extending to approximately the same depth beneath the first surface, further wherein the separation region defines a generally flat plane.

51. The substrate of claim 42, further comprising:

a first operable microelectronic device in a first die portion at and/or proximate to the first surface of the substrate body; and

a second operable microelectronic device in a second die portion at and/or proximate to the first surface of the substrate body, the second die portion being separable from the first die portion.

52. A microelectronic substrate, formed by the process comprising:

providing a substrate having a first surface and a second surface facing a direction opposite from the first surface;

forming a plurality of voids in the substrate, each void extending from the first surface to a separation region between the first and second surfaces;

forming at least one operable microelectronic device at and/or proximate to the first surface of the substrate; and

separating a first stratum of the microelectronic substrate above the separation region from a second stratum of the microelectronic substrate below the separation region.

53. The substrate of claim 52 wherein forming the first stratum includes forming the first stratum to have a thickness of less than about 150 microns measured from the first surface to the separation region.

54. The substrate of claim 52, further comprising:

at least partially filling the voids with a filler material to close an open end of the voids at the first surface of the substrate;

disposing a film on the first surface of the substrate; and

forming the microelectronic device in the film.

55. The substrate of claim 52 wherein forming the voids includes forming tapered voids having a first void area transverse to the first surface of the substrate at the first surface and a second void area transverse to the first surface of the substrate below the first surface, the second void area being larger than the first void area.

56. The substrate of claim 52, further comprising forming the voids to have approximately the same depth beneath the first surface so that the separation region is generally flat.

57. The substrate of claim 52, further comprising closing entrance openings of the voids at the first surface of the substrate by at least partially filling the voids.

58. The substrate of claim 52 wherein forming the voids includes forming tapered voids by disposing an etchant on the first surface of the substrate and tilting the substrate.

59. The substrate of claim 52 wherein forming the voids includes forming tapered voids by directing an energy beam toward the first surface of the substrate and tilting the substrate as the energy beam impinges on the first surface.

60. The substrate of claim 52, further comprising spacing adjacent voids by a distance less than a transverse dimension of a die formed from the substrate.

61. The substrate of claim 52 wherein separating the first stratum of the microelectronic substrate from the second stratum includes applying a force in a selected

direction to the first stratum to break connecting portions of the microelectronic substrate coupling the first and second strata of the microelectronic substrate between the voids.

62. The substrate of claim 61, further comprising varying a magnitude of the force while engaging the first stratum of the microelectronic substrate.

63. The substrate of claim 61 wherein applying a force includes applying a force in a direction parallel to a plane of the separation region.

64. The substrate of claim 61 wherein applying a force includes applying a force transverse to a plane of the separation region.

65. The substrate of claim 61, further comprising releasably engaging the first surface of the substrate by applying a suction force to the first surface.

66. The substrate of claim 52 wherein forming at least one microelectronic device includes forming first microelectronic devices defining a first microelectronic die and forming second microelectronic devices defining a second microelectronic die.

67. The device of claim 52, further comprising selecting the substrate to include a silicon wafer.

68. The device of claim 67, further comprising selecting the wafer to have a diameter of from about eight inches to about twelve inches.